A 5 TO 10GHz LOW SPURIOUS TRIPLE TUNED TYPE PLL SYNTHESIZER DRIVEN BY FREQUENCY CONVERTED DDS UNIT

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ABSTRACT

This paper presents a 5 to 10GHz low spurious triple tuned type PLL synthesizer with narrow channel steps for wide-band reception in RF measurement systems. The synthesizer is driven by a DDS to achieve such characteristics with a single PLL configuration. It corrects DDS's output frequency and division ratios of two variable frequency dividers in the PLL. With the proposed topology, high level spurious components by the DDS do not fall in from the PLL's loop bandwidth. An added frequency converter placed between the DDS and PLL also suppresses spurious level by reducing a transfer gain from the DDS to the PLL output. Furthermore, a voltage controlled oscillator (VCO) with inverted tuning circuits is presented for low phase noise characteristics. A developed PLL synthesizer with channel step 625kHz achieved low spurious level below -46dBc, phase noise of -105dBc/Hz @1MHz offset and switching speed of 90 ˚s.

I. INTRODUCTION

A frequency synthesizer is often employed for a wide-band reception in RF measurement systems[1]. In such systems, requirements for the synthesizer are, (a) wide-band and narrow channel steps, (b) low phase noise and low spurious level and (c) fast frequency switching speed[2]. Analog direct synthesizers[1] are generally employed in such systems, because they can achieve these requirements. They however consist of many components, so their sizes are extremely large. On the other hand, PLL synthesizers can achieve small size easily, thus they are employed in many communication systems. But, the PLL synthesizer cannot achieve low phase noise and fast switching speed when its reference frequency becomes low at narrow channel step.

The PLL synthesizer driven by a direct digital synthesizer (DDS)[3]-[6] can achieve narrow channel step without a degradation of frequency switching speed and phase noise, since the DDS produces frequency with milli-Hz order resolution by digital calculations. However, there are spurious components due to quantization errors of digital calculations and nonlinearity of a digital to analog converter[7]. The PLL is unable to suppress these components when they exist in the PLL's loop bandwidth. So, this synthesizer is not generally used in microwave-region for this reason.

This paper presents a 5 to 10GHz low spurious triple tuned type PLL synthesizer driven by a frequency converted DDS unit for RF measurement systems. The synthesizer determines an appropriate value of output frequency of the DDS and division ratios of two variable frequency dividers in the PLL to avoid high level spurious components falling in the PLL's loop bandwidth. The added frequency converter also suppresses spurious level by reducing a transfer gain from the DDS to the PLL output. Moreover, a VCO with two inverted series resonators is also employed to achieve wide-band and low phase noise at the same time.

II. CONFIGURATION

A. PLL SYNTHESIZER

Figure 1 indicates a configuration of the triple tuned type PLL synthesizer with the frequency converted DDS unit. Output frequency of the DDS (f_d) is converted to reference frequency of the PLL (f_r) by a mixer and variable frequency divider 1 (VFD1). Output frequency of the PLL (f_o) is given as follows:

$$f_o = \left(\frac{N}{R}\right)\cdot\left(f_{ck} + f_d\right),\ f_d = \frac{k \cdot f_{ck}}{2^L} \qquad (1)$$

where R and N are frequency division ratios of the VFD1 and VFD2 respectively, f_{ck} is a clock frequency of the DDS, k is a frequency setting data of the DDS, L is a word length of k (We consider only the case of $k<2^{L-1}$). The synthesizer sets fine frequency tuning of f_o by altering k, and coarse frequency tuning of f_o by altering N and R. The values of k, N and R are determined to avoid high level spurious components from the PLL's loop bandwidth, and are saved in a ROM. Calculation method for determining of k, N and R is described in more detail in section III.

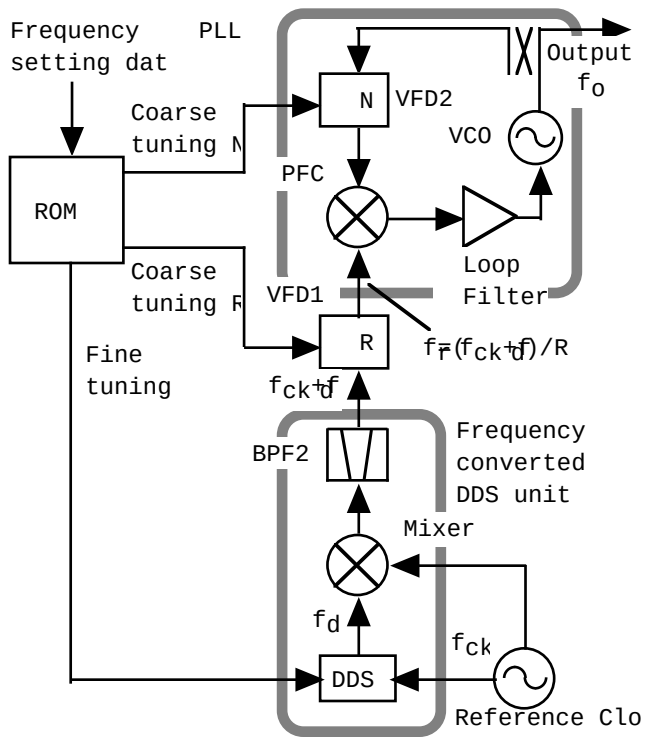

Fig.1. Triple tuned type PLL synthesizer with the frequency converted DDS unit (Triple tuning topology and frequency converted DDS unit are proposed for low spurious characteristics.)

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B. VCO

Figure 2 indicates a configuration of the VCO with two inverted series resonators. Tuning circuits are added to source and gate terminals of GaAs FFT. Each tuning circuit is made of series resonator (consisting of inductor and varactor diode) and inverter. The inverter increases loaded Q of the tuning circuit to reduce phase noise of the VCO. These two inverters are designed to have different center frequencies (f_1 and f_2 in the figure) to achieve wide-band oscillation.

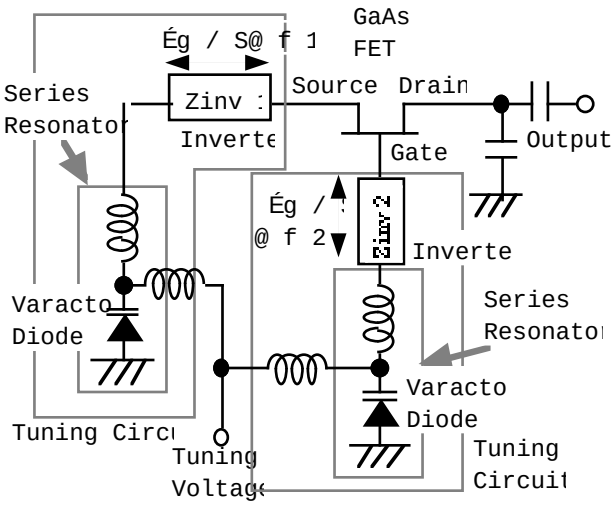


Fig.2. VCO with two inverted series resonators (f_1 and f_2 are different frequencies to achieve wide-band oscillation.)

III. DESIGN THEORY OF TRIPLE TUNED TYPE SYNTHESIZER

A. SPURIOUS COMPONENTS

Frequency of a spurious component of the DDS (f_{dsp}) is given by f_d and f_{ck} as follows[6]:

$$f_{dsp} = \left| m \cdot f_d - n \cdot f_{ck} \right| \tag{2}$$

where m and n are harmonic numbers. Figure 3 indicates measured spurious levels versus harmonic number m. As shown in the figure, S_{dsp} becomes lower as m becomes larger. Thus, a frequency setting for achieving low spurious level can be accomplished by designing spurious components of lower m to not fall in the PLL's loop bandwidth. Frequency range of the spurious component which fall in the PLL's loop bandwidth is $f_{dsp}<0.5f_{ck}$, since the frequency range of f_d is also less than $0.5f_{ck}$. Using the relationship $f_{dsp}<0.5f_{ck}$, the value of n can be determined from m, f_d and f_{ck}, and is replaced from eq.(2). Now, f_{dsp} becomes as follows:

$$f_{dsp} = \left| m \cdot f_d - \mathrm{round}\left[\frac{m \cdot f_d}{f_{ck}} \right] \cdot f_{ck} \right| \tag{3}$$

where round[] is a function that rounds off a number to an integer. The condition whether high level spurious component exists in the PLL's loop bandwidth is given as follows:

$$B_L > \left| f_d - f_{dsp} \right| = \left| (m \pm 1) \cdot f_d - \mathrm{round}\left[\frac{m \cdot f_d}{f_{ck}} \right] \cdot f_{ck} \right| \tag{4}$$

where B_L is the PLL's loop bandwidth.

First, N is determined from a provisional value of R and k by eq.(1). Then k is recalculated from R and N. Finally, using eq.(3) and (4) to determine whether high level spurious components are in the PLL's loop bandwidth or not. If it is so, R is varied, then k and N are recalculated. This parameter setting process continues until all of high level spurious components do not fall in the PLL's loop bandwidth. By the proposed topology, spurious level of the PLL synthesizer driven by the DDS can be suppressed.

Level of the spurious component in the PLL's loop bandwidth at output of the PLL S_{out} is given as follows:

$$S_{out} \cong \left(\frac{f_o}{f_{ck} + f_d} \right)^2 \cdot S_{dsp} \tag{5}$$

By eq.(5), S_{out} can be reduced with large f_d or f_{ck}. But, there is an upper limit of f_d because f_d is decided by the DDS operating frequency. The proposed synthesizer can reduce S_{out} by employing the frequency converted DDS unit consisting of the mixer with large f_{ck}.

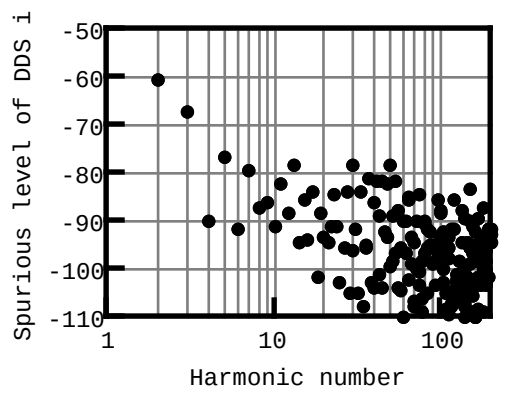


Fig.3. Measured spurious level versus harmonic number m of the DDS(Phase resolution:14bits, Amplitude resolution:10bits).

B. PHASE NOISE

Phase noise at the output of the PLL synthesizer $L_{out}(j\ Ö)$ is given as follows:

$$L_{out}(j\omega) \cong \left(\frac{f_o \cdot R}{f_{ck} + f_d} \right)^2 \cdot \left| H_n(j\omega) \right|^2 \cdot L_{lp}(j\omega) + \left| 1 - H_n(j\omega) \right|^2 \cdot L_{vco}(j\omega) \tag{6}$$

where $L_{lp}(j\ Ö)$ is noise due to components of the PLL, $L_{vco}(j\ Ö)$ is phase noise due to the VCO, $H_n(j\ Ö)$ is the PLL's closed loop transfer function which is normalized by N. In the pass-band of the PLL, $H_n(j\ Ö)$ is approximated by 1, then the first term of eq.(6) becomes dominant. As already shown in section III.A, higher f_{ck} for low spurious level also reduces $L_{out}(j\ Ö)$ since the first term of eq.(6) is lowered. Outside the pass-band, $H_n(j\ Ö)$ is approximated by 0, then the second term is dominant. Thus $L_{out}(j\ Ö)$ depends on $L_{vco}(j\ Ö)$. The VCO with two inverted series resonators is developed to reduce $L_{vco}(j\ Ö)$.

IV. 5 to 10GHz PLL SYNTHESIZER

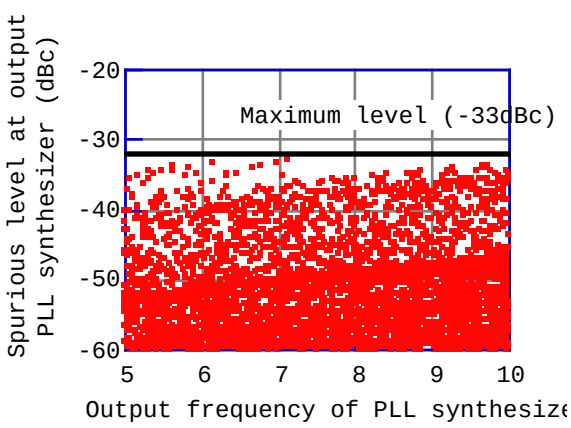
A. DESIGN RESULTS

Table 1 indicates a parameter summary for a developed 5 to 10GHz PLL synthesizer. The DDS has spurious characteristic shown in Figure 3. R is varied by }1 to recalculate k and N, then high level spurious components are

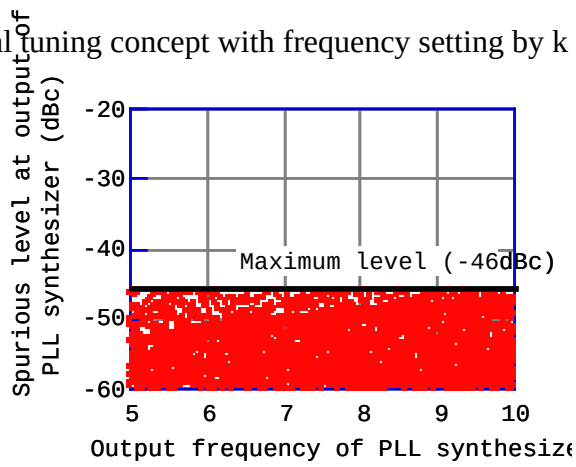
avoided from the PLL's loop bandwidth. Figure 4 indicates calculated spurious levels of the PLL synthesizer. Figure 4(a) shows calculated results by the dual tuning concept[6] with frequency setting by k and N not by R. Figure 4(b) shows calculated results by the triple tuning concept with frequency setting by k, N and R. If the triple tuning concept is adapted, spurious level of the synthesizer is expected to be reduced by 13dB compared with the dual tuning concept.

Table 1. parameter summary

Range of f_o	5 to 10GHz
Channel step of f_o	0.625MHz
Tuning range of R	}1
Reference frequency of f_r	8MHz
Natural frequency of the	100kHz
Spurious level	below -46dBc



(a) dual tuning concept with frequency setting by k and N



(b) triple tuning concept with frequency setting by k, N and R

Fig.4. Calculated spurious levels of the PLL synthesizer.

B. MEASUREMENT RESULTS

Figure 5 indicates a photograph of a developed VCO module. The VCO is fabricated on alumina ceramic substrates of 0.25mm thickness. The VCO module size is 9.6mm ~ 16.4mm. This VCO employs GaAs FET with gate width of 800 ˚m and GaAs hyper-abrupt varactor diodes for low loss tuning circuits. Figure 6 indicates measurement results of oscillating frequency and phase noise of the developed VCO. A range of oscillating frequency from 4.88 to 10.11GHz and phase noise below -116dBc/Hz@1MHz are obtained. This is regard as one of the lowest values compared with past works[8]. Figure 7 indicates measured spurious levels of the PLL synthesizer. In the figure, a dotted line indicates minimum values which are determined by integrated noise of developed synthesizer and resolution bandwidth of spectrum analyzer used in measurements. The maximum value of S_{out} is -46dBc and is nearly equal to the calculated value. Therefore, the effect of the triple tuning concept is suppression of spurious level by 13dB, and it is in good agreement with design results. Figure 8 indicates an output spectrum of the synthesizer at f_o=5GHz, and Figure 9 indicates measured phase noise of the synthesizer. Phase noise is -105dBc/Hz@1MHz. Phase noise in the loop bandwidth of -83dBc/Hz gives integrated phase noise of about -33dBc/100kHz. Thus spurious level is negligibly small compared with integrated phase noise. Figure 10 indicates a transient response of the PLL synthesizer. The frequency switching speed is 90 ˚s with frequency error of 1MHz.

By measurement results, the developed small sized single PLL synthesizer can achieve wide-band, narrow channel step and fast frequency switching speed with low spurious and phase noise characteristics.

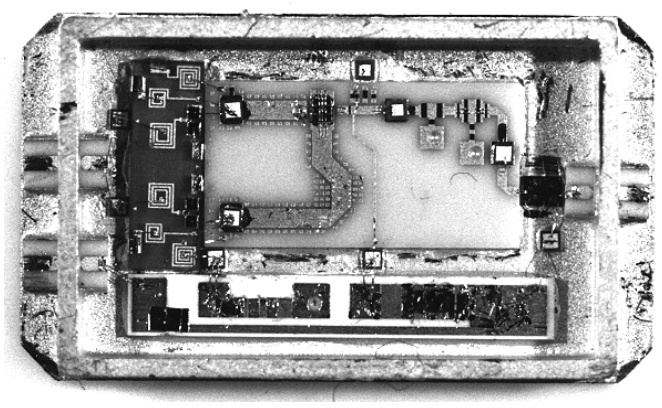


Fig. 5. Photograph of a developed VCO module (module size: 9.6mm ~ 16.4mm).

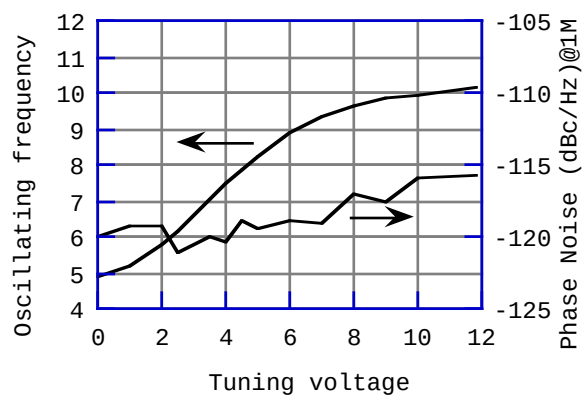


Fig.6. Measurement results of oscillating frequency and phase noise of the developed VCO.

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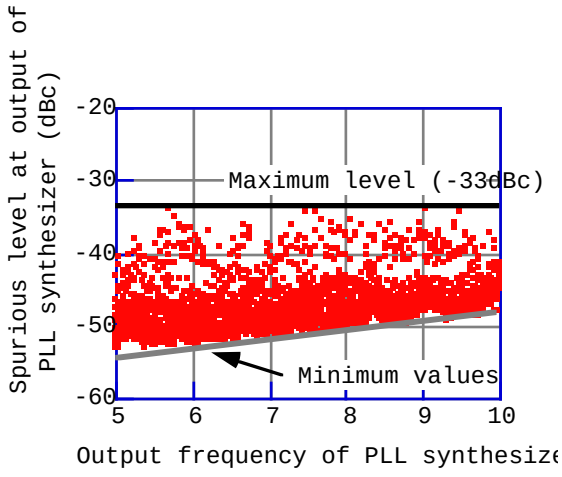
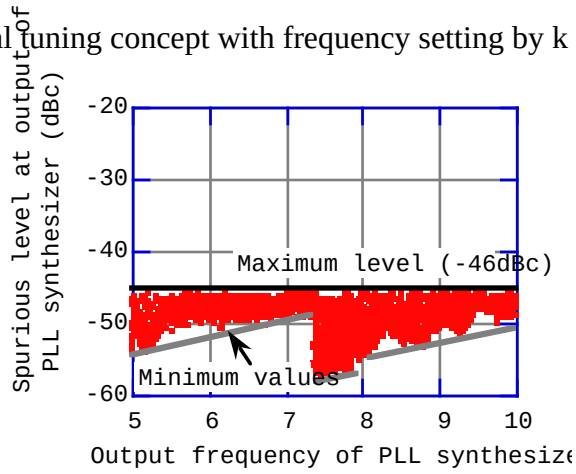


(a) dual tuning concept with frequency setting by k and N



(b) triple tuning concept with frequency setting by k, N and R

Fig.7. Measured spurious levels of the PLL synthesizer. Minimum values are determined by integrated noise of developed synthesizer and resolution bandwidth of spectrum analyzer used in measurements.

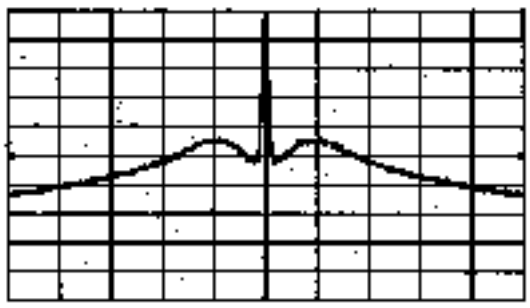


Fig.8. Output spectrum of the synthesizer at f_o=5GHz (Ver. :10dB/div, Hori. :100kHz/Div, RBW: 3kHz).

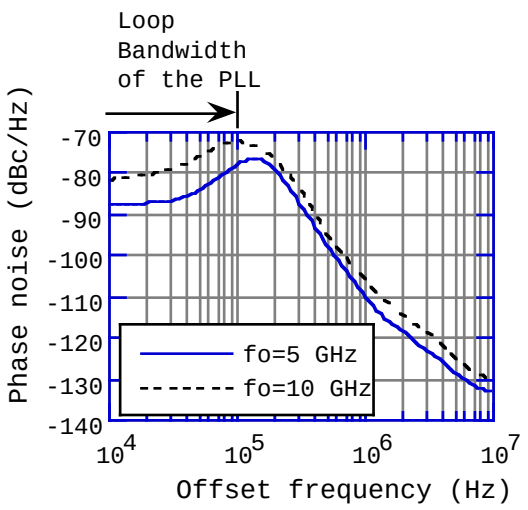


Fig.9. Measured phase noise of the synthesizer.

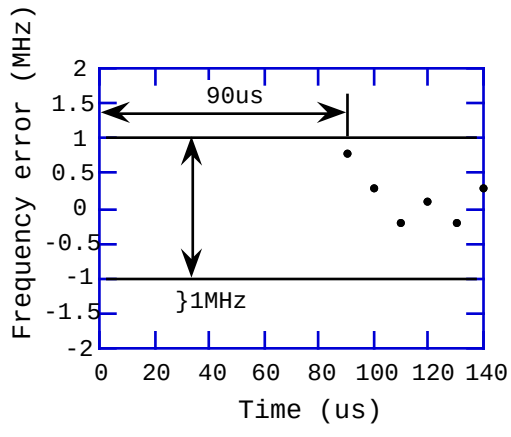


Fig.10. Transient response of the PLL synthesizer (f_o is changed from 5GHz to 10GHz).

V. CONCLUSION

A 5 to 10GHz wide-band PLL synthesizer was developed for RF measurement systems. Triple tuning concept and frequency converted DDS unit were applied for achieving low spurious characteristic of the synthesizer. The VCO with two inverted series resonators was used for reducing phase noise. A developed 5 to 10GHz PLL synthesizer with channel step 625kHz can achieve spurious level below -46dBc, phase noise of -105dBc/Hz@1MHz offset and switching speed of 90 ˚s. These results are suitable for wide reception in the RF measurement systems.

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